IN THE CLAIMS:

Claims 3, 9, 10, 11, 13, 19-21, 23, 29-31, 33, and 35 have been amended herein. All of the pending claims 1 through 38 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Original) A circuit for reducing power during a standby mode of a memory device, comprising:

a reference including at least first and second reference signals;

a switching device including at least first and second switching inputs respectively coupled to the at least first and second reference signals and a switching output configured to toggle from outputting the first reference signal to outputting the second reference signal during a standby mode; and

a first regulator coupled and responsive to the switching output of the switching device, the first regulator configured to output a first internal operational power derived from an external operational power as regulated by one of the first and second reference signals.

2. (Original) The circuit of claim 1, wherein the reference is a voltage divider including at least first and second taps corresponding to the at least first and second reference signals.

3. (Currently Amended) The circuit of claim 1, wherein the switching device comprises a multiplexer including ~~at~~ the at least first and second switching inputs, ~~an~~ the switching output and control inputs responsive to the standby mode.

4. (Original) The circuit of claim 1, further comprising a second regulator coupled and responsive to at least one of the first and second reference signals, the second regulator configured to output a second internal operational power isolated from the first internal operational power.

5. (Original) The circuit of claim 4, wherein the second regulator is coupled and responsive to the first reference signal.

6. (Original) The circuit of claim 4, wherein the second regulator is coupled and responsive to the switching output.

7. (Original) The circuit of claim 1, wherein the standby mode is a self-refresh mode of memory cells within a dual data rate memory device.

8. (Original) The circuit of claim 1, wherein the standby mode is a power-down mode of memory cells within a dual data rate memory device.

9. (Currently Amended) The circuit of claim 1, wherein the first reference signal corresponds to a regulation of the first internal operational power ~~signal VCCR~~ to approximately 2.0 volts.

10. (Currently Amended) The circuit of claim 9, wherein the second reference signal corresponds to a regulation of the first internal operational power ~~signal VCCR~~ to approximately 1.5 volts.

11. (Currently Amended) A memory device comprising:

a memory array including at least one memory cell configured to be periodically refreshed;

control logic coupled to the memory array and responsive to mode commands from a memory controller;

a circuit for reducing power during a standby mode of the mode commands, including:

a reference including at least first and second reference signals;

a switching device including at least first and second switching inputs respectively coupled to the at least first and second reference signals and a switching output

configured to toggle from outputting the first reference signal to outputting the second reference signal during ~~a~~ the standby mode; and

a first regulator coupled and responsive to the switching output of the switching device, the first regulator configured to output a first internal operational power derived from an external operational power as regulated by one of the first and second reference signals.

12. (Original) The memory device of claim 11, wherein the reference is a voltage divider including at least first and second taps corresponding to the at least first and second reference signals.

13. (Currently Amended) The memory device of claim 11, wherein the switching device comprises a multiplexer including ~~at~~ the at least first and second switching inputs, ~~an~~ the switching output and control inputs responsive to the standby mode.

14. (Original) The memory device of claim 11, further comprising a second regulator coupled and responsive to at least one of the first and second reference signals, the second regulator configured to output a second internal operational power isolated from the first internal operational power.

15. (Original) The memory device of claim 14, wherein the second regulator is coupled and responsive to the first reference signal.

16. (Original) The memory device of claim 14, wherein the second regulator is coupled and responsive to the switching output.

17. (Original) The memory device of claim 11, wherein the standby mode is a self-refresh mode of memory cells within a dual data rate memory device.

18. (Original) The memory device of claim 11, wherein the standby mode is a power-down mode of memory cells within a dual data rate memory device.

19. (Currently Amended) The memory device of claim 11, wherein the first reference signal corresponds to a regulation of the first internal operational power ~~signal VCCR~~ to approximately 2.0 volts.

20. (Currently Amended) The memory device of claim 19, wherein the second reference signal corresponds to a regulation of the first internal operational power ~~signal VCCR~~ to approximately 1.5 volts.

21. (Currently Amended) An electronic system including an input device, an output device, a memory device, and a processor device coupled to the input, output, ~~and a~~ and memory ~~device~~ devices, the memory device comprising:

a memory array including at least one memory cell configured to be periodically refreshed;

control logic coupled to the memory array and responsive to mode commands from a memory controller;

a circuit for reducing power during a standby mode of the mode commands, including:

a reference including at least first and second reference signals;

a switching device including at least first and second switching inputs respectively coupled to the at least first and second reference signals and a switching output configured to toggle from outputting the first reference signal to outputting the second reference signal during ~~a~~ the standby mode; and

a first regulator coupled and responsive to the switching output of the switching device, the first regulator configured to output a first internal operational power derived from an external operational power as regulated by one of the first and second reference signals.

22. (Original) The electronic system of claim 21, wherein the reference is a voltage divider including at least first and second taps corresponding to the at least first and second reference signals.

23. (Currently Amended) The electronic system of claim 21, wherein the switching device comprises a multiplexer including ~~at~~ the at least first and second switching inputs, ~~an~~ the switching output and control inputs responsive to the standby mode.

24. (Original) The electronic system of claim 21, further comprising a second regulator coupled and responsive to at least one of the first and second reference signals, the second regulator configured to output a second internal operational power isolated from the first internal operational power.

25. (Original) The electronic system of claim 24, wherein the second regulator is coupled and responsive to the first reference signal.

26. (Original) The electronic system of claim 24, wherein the second regulator is coupled and responsive to the switching output.

27. (Original) The electronic system of claim 21, wherein the standby mode is a self-refresh mode of memory cells within a dual data rate memory device.

28. (Original) The electronic system of claim 21, wherein the standby mode is a power-down mode of memory cells within a dual data rate memory device.

29. (Currently Amended) The electronic system of claim 21, wherein the first reference signal corresponds to a regulation of the first internal operational power ~~signal VCCR~~ to approximately 2.0 volts.

30. (Currently Amended) The electronic system of claim 29, wherein the second reference signal corresponds to a regulation of the first internal operational power ~~signal VCCR~~ to approximately 1.5 volts.

31. (Currently Amended) An integrated circuit die comprising:

a memory array including at least one memory cell configured to be periodically refreshed;

control logic coupled to the memory array and responsive to mode commands from a memory controller;

a circuit for reducing power during a standby mode of the mode commands, including:

a reference including at least first and second reference signals;

a switching device including at least first and second switching inputs respectively coupled to the at least first and second reference signals and a switching output configured to toggle from outputting the first reference signal to outputting the second reference signal during ~~a~~ the standby mode; and

a first regulator coupled and responsive to the switching output of the switching device, the first regulator configured to output a first internal operational power derived from an external operational power as regulated by one of the first and second reference signals.

32. (Original) The integrated circuit die of claim 31, wherein the reference is a voltage divider including at least first and second taps corresponding to the at least first and second reference signals.

33. (Currently Amended) The integrated circuit die of claim 31, wherein the switching device comprises a multiplexer including ~~at~~ the at least first and second switching inputs, ~~an~~ the switching output and control inputs responsive to the standby mode.

34. (Original) The integrated circuit die of claim 31, further comprising a second regulator coupled and responsive to at least one of the first and second reference signals, the second regulator configured to output a second internal operational power isolated from the first internal operational power.

35. (Currently Amended) A semiconductor wafer including an integrated circuit comprising:

a memory array including at least one memory cell configured to be periodically refreshed;

control logic coupled to the memory array and responsive to mode commands from a memory controller;

a circuit for reducing power during a standby mode of the mode commands, including:

a reference including at least first and second reference signals;

a switching device including at least first and second switching inputs respectively coupled to the at least first and second reference signals and a switching output configured to toggle from outputting the first reference signal to outputting the second reference signal during ~~a~~ the standby mode; and

a first regulator coupled and responsive to the switching output of the switching device, the first regulator configured to output a first internal operational power derived from an external operational power as regulated by one of the first and second reference signals.

36. (Original) A method for reducing power during a standby mode of a memory device, comprising:

switching from a higher reference signal to a lower reference signal as an output reference signal during a standby mode of a memory device; and

regulating a first lower internal operation power from an external operational power in response to the output reference signal during the standby mode, the first lower

internal operational power for operating at least a first portion of the memory device during a duration of the standby mode.

37. (Original) The method of claim 36, wherein switching comprises multiplexing between the higher reference signal and the lower reference signal in response to the standby mode.

38. (Original) The method of claim 36, further comprising further regulating a second lower internal operation power from an external operational power in response to the output reference signal during the standby mode, the second lower internal operational power for operating at least a second portion of the memory device during a duration of the standby mode.